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STRATEGIES FOR REDUCING POWER CONSUMPTION DURING IC TESTING: POWER-AWARE DFT IN PRACTICE

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ABSTRACT
In order to verify the functionality, performance, and dependability of semiconductor devices, IC testing is a crucial requirement. High consumption of energy used in carrying out tests subjects the devices to thermal stresses, affecting the reliability of the devices besides driving up the manufacturing expenses incurred by semiconductor manufacturers. This article discusses comprehensive designs with full fault detection capabilities. The article looks at six main methods: clock gating, which turns off unused parts of a circuit; partitioned testing, which divides large designs for easier analysis; test data compression, which lessens the activity of scan chains; voltage management, which improves power supply during testing; dynamic voltage and frequency scaling, which adjusts to different workload needs; and enhanced scan chain optimization, which reduces unnecessary signal changes. All these methodologies afford an answer to thermal issues, increase the lifespan of these devices, cut the cost of production, and minimize environmental degradation by using less energy. The strategies offer realistic implementation systems, which can be used on a wide range of integrated circuit structures encompassing mobile processors, automotive electronics, and high-performance computing systems. Future plans include combining machine learning to create patterns, managing power use in different designs, and setting industry-wide standards for power-aware Design for Test practices.

Keywords: Power-Aware Design For Test, Integrated Circuit Testing, Dynamic Power Reduction, Test Pattern Optimization, Low-Power Test Methodologies

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1. Introduction

The semiconductor industry has experienced significant advances in the complexity of integrated circuits, and the current devices have billions of transistors running at geometries of nanometers. This technological innovation has radically changed the way integrated circuit testing is done and is bringing about significant issues in power management, which were insignificant with other technology generations [1]. Power consumption in integrated circuit testing has become a major issue of concern to semiconductor companies not only in terms of economics of production but also in terms of reliability of devices and environmental sustainability. The increasing power needs during testing come from the higher number of transistors packed into designs, faster operating speeds, and the more complex functions of today's integrated circuits.

Beyond the immediate energy costs, the issue of excessive power consumption during testing activities has negative consequences. Local heating effects due to high power dissipation during test operations may cause thermal problems, which may result in damage to the semiconductor devices or change their electrical characteristics. These thermal loads are even more challenging in the more advanced process nodes with smaller feature sizes and higher power densities [2]. Loss of reliability of the device occurs when the testing procedure exposes circuits to a level of power beyond their design capacity that may cause latent defects that become apparent during the practical deployment. There are escalated operation expenses in manufacturing plants in terms of cooling arrangements, power supply systems, and long testing durations to deal with thermal limitation in testing processes [11].
Conventional testing methodologies, which are designed with the main aim of maximizing fault coverage and reducing test time, may not work well in the fight against power consumption. Traditional scan-based test methods stimulate entire circuits at the same time, generating switching patterns that are much larger than typical patterns of operation [3]. Algorithms of automatic test pattern generation in the past were mainly focused on fault detection efficiency and not power implications; hence, the test sequences have very high power requirements for the devices being tested. The imbalance of old model testing and contemporary power limitations would demand some radical alterations in Design for Test.

Power-aware Design for Test Methods represents a necessary change to semiconductor testing habits [1]. These strategies recognize that managing test power should not be an afterthought during production or product design. Power-aware Design approaches to testing consider conflicting goals of ensuring high fault coverage, minimizing test application time, and limiting power consumption to acceptable limits. The application of these methodologies will be achieved through a coordinated effort in the areas of test pattern generation, design-for-test architecture selection, and optimization of test schedules.

The article covers both software algorithmic development and hardware architectural development [2]. The methods talked about include clock gating, which turns off parts of the circuit that aren't in use; testing large systems in smaller parts; reducing the amount of test data to save energy; controlling voltage for better power supply; adjusting the voltage and frequency based on workload; and improving scan chains to reduce unnecessary signal changes. All these strategies give the complete solution to power management challenges in modern integrated circuit testing.
The next sections will cover the basic ideas of power use in testing, how each power-saving method works, practical issues when using them in industry, and what the future might hold for these energy-saving testing methods. The frameworks above provide semiconductor manufacturers with practical advice on how to institute power-saving testing processes that can save energy and cut off the related costs without compromising quality.

2. Fundamentals of Power Consumption in IC Testing

The power used in testing integrated circuits comes from two main factors that determine how energy is lost in complementary metal-oxide-semiconductor circuits. The biggest part of power used during testing comes from dynamic power consumption, which happens when the circuit nodes charge and discharge due to changes in signals. Leakage currents through transistors when the circuit is stable add to the total power use, and this increase is happening because of today's technologies that use lower threshold voltages and thinner gate oxides. The correlation between these elements of power dictates the total energy requirements in the testing processes, wherein dynamic power usually prevails in the test processes since scan-based testing processes are characterized by intensive switching processes [6].

Too much power is used during testing because the testing conditions are different from how the circuit normally works, causing many parts of the circuit to switch on and off at the same time. The scan chain loading can be followed by capture, which can lead to simultaneous changes in many circuit parts, resulting in temporary spikes in

power that can strain the power delivery systems. Test pattern sequences created to optimize fault coverage can activate circuit portions that almost never activate simultaneously during normal operation.

Switching activity is the biggest cause of power loss during testing, and the amount of power used increases with the number of times signals change between circuit points. The charge or discharge of nearby parasitic capacitances during each signal change is necessary. The correlation between these power components determines the total energy requirements during testing processes, where dynamic power typically dominates due to the intensive switching associated with scan-based testing methods [6].Test pattern optimization methods are also aimed at minimizing switching activity by attentively choosing test vector sequences that meet the desired fault coverage as well as minimizing redundant signal transitions.

Thermal limitations severely constrain the testing processes, as the high concentration of power dissipation causes local heating effects. Temperature variations in integrated circuits during testing may be much higher than those experienced when operating under functional conditions and may result in thermal stress-related failures or irreversible damage to a device [6]. Junction temperatures are raised, which promotes the degradation processes such as electromigration and hot carrier injection, as well as time-dependent dielectric breakdown, which poses a challenge to the reliability of long-term operation of the device. The testing processes must maintain the die temperatures within a specific range to ensure accurate fault detection without reducing production quality due to heat, which can happen with slower test clock rates or energy-saving testing methods.

Noise of power supply when high switching test conditions occur can cause voltage drops, which create timing violations or functional errors, creating test escapes where faulty devices pass validation. Concurrent switching activity structures electromagnetic interference and couples into some sensitive analog circuits, or input/output structures, to form noise margins that are detrimental to test accuracy [12].

Essential circuits orfs in the development of test strategies exist due to the relationship between the requirements of test coverage and the requirements of power. Full fault coverage requires test patterns that exercise a wide range of circuit paths and circuit operational states, thus necessitating a wide range of switching activities that are power consuming in nature [6]. The classical methods focused on maximizing the coverage without energy limitations and tolerated high energy consumption as an inevitable condition to the quality assurance. The contemporary approach to power consciousness acknowledges that coverage and power goals do not have to oppose each other, when power administration is taken into account in the early-stage testing strategies, as opposed to thinking of power as an additional factor that is considered after the covering goals have been set.

3. Clock Gating and Partitioned Testing Techniques

Clock gating is an important technique for minimizing dynamic power usage in the testing of integrated circuits by disabling clock gates to idle circuitry. This method takes advantage of the fact that the test patterns normally only use portions of the circuit functionality at any one time, and large portions of the design are idle during a particular test condition [1]. The basic idea is to place gating logic that prevents the clock from propagating to parts of the circuit that are not under active test operation, which removes the unnecessary switching activity in these parts of the circuit, achieving power reductions of up to 96% during scan loading operations and 87% during scan unloading phases [2]. It has to be implemented with close consideration of the behavior of test patterns to find out areas where the circuit partitions may be left in an inactive state safely without interfering with fault detection functions.

The design of the pattern test is vital in the enhancement of the clock gating effectiveness during testing processes. Patterns should be designed in such a way that only the required parts of the circuit are activated and idle modules are kept in gated states, and as such synchronization between automatic test pattern generation algorithms and clock gating control logic is necessary [2]. The gating control signals are based on the content of the test pattern, and they allow the dynamic control of the circuit regions to be activated and deactivated as testing advances to new fault coverage goals. The method is in contrast to functional mode clock gating which reacts to data-dependent patterns of activity, whereas test mode gating is based on known schedules in sync with test sequence arrangement.

Gated testing implementation systems include software toolchains and hardware architectural changes. Hardware portions and components consist of clock gating cells placed at key hierarchy points, control logic that decodes test patterns and provides gating signals, and scan chain adjustments to enable independent control of partitions of the circuit, demonstrating a 70% average reduction and a 32% peak reduction in capture operations [3]. The software

needs to be improved to compute the circuit topology, determine the appropriate gating boundaries, produce the right test patterns that consider gating constraints, and ensure that the objectives of fault coverage are met even with lower switching activity. The combination of this software and hardware doesn't only result in extensive testing environments that achieve significant power savings and quality standards.

Partitioned testing methodologies solve the problem of power management of large integrated circuit designs by splitting devices into smaller portions which are tested during separate phases [1]. This segmentation plan acknowledges that the instantaneous power requirements of simultaneous testing of entire chips are above both design and tester limits in the advanced technology nodes. Functional module boundaries are commonly aligned with partition boundaries, clock domain or power domain boundaries, which can be used to divide into natural partitions that reduce dependencies between partitions during testing. The individual partitions are given test patterns of their own, in a sequence where power consumption at any given time is kept less than manageable limits [13].

Independent module testing strategies allow control of power distribution to be finely controlled when applying the test. Because of the sequential activation of partitions, cumulative power demand would not occur, which would otherwise be caused by simultaneous testing of all modules, but this causes power consumption to be spread across long intervals of the test instead of being concentrated in short periods of high power usage [2]. This time distribution keeps average power within reasonable limits and allows complete fault coverage of all partitions. Intelligent clock gating implementations exhibit frequency-dependent behavior, with power savings of 44.9% at 100 MHz scaling up to 65.6% at 1 GHz operation [3]. The results in test time overhead by using sequential partition testing, providing tradeoffs between power management goals and test duration, which needs to be determined based on manufacturing needs.

Partition management helps lower peak power by stopping hot spots from forming, which is a big problem in tightly packed integrated circuits because they can overheat and get damaged or become less reliable. Partitioned testing will guarantee that active circuit areas are not working at the same time and the thermal loads are spatially distributed within the die. This arrangement of space helps to spread out the power usage over time, creating a full control over heat that protects the equipment during testing and also allows for thorough checking of all parts of a circuit.

Technique	Test Operation	Power Reduction (%)
Clock Gating Cells	Scan Loading	96
Clock Gating Cells	Scan Unloading	87
Clock Gating Cells	Average Capture	70
Clock Gating Cells	Peak Capture	32
Intelligent Clock Gating (100 MHz)	Dynamic Power	44.9
Intelligent Clock Gating (500 MHz)	Dynamic Power	44.8
Intelligent Clock Gating (1000 MHz)	Dynamic Power	65.6

Table 1: Clock Gating Power Reduction Comparison [2, 3]

The quantitative results show considerable power reduction in the use of clock gating methodologies at the testing stages. Scan loading is reduced by 96%, and scan unloading is reduced by 87% using the clock gating cells [2]. The average reduction and 96% reduction are considered 70% and 32% in capture operations, respectively. The intelligent clock gating has a frequency-dependent behavior with an estimated saving of 44.9% at 100 MHz and increases with frequency to 65.6% at 1 GHz of operation [3]. These empirical results verify that clock gating is a useful tool in the management of dynamic power when running a test.

4. Test Data Compression and Pattern Optimization

The principles of compressed test data are essential in the resolution of power consumption because the volume of information that is transferred by the scan chains during testing operations is reduced. The compression method acknowledges that test patterns have a high level of redundancy, and there is a large number of bit positions that are set to don't-care values and which do not affect the results of fault detection [8]. Encoding schemes take advantage of this redundancy to encode test data in small forms, decreasing the number of scan shifts needed to load patterns into test circuits. The shift operation decrease is directly proportional to a decrease in switching operation since the

number of transitions is reduced during the scan chain loading operations that consume the majority of power in scan-based testing systems.

The methods used in reducing the volume of scan chain data use different encoding methods to attain compression ratios that can dramatically reduce the test data requirements. Run-length encoding records a sequence of like bit values in compressed codes, achieving compression ratios between 53.37% and 85. 55% depending on circuit characteristics, whereas statistical codes assign shorter codes to common patterns [8, 9]. The method based on dictionaries keeps libraries of pattern fragment segments, and these segments are identified by short indices instead of sending entire bit sequences. The choice of suitable compression methodology depends on the properties of patterns, where various techniques have mentioned some benefits of specific test data distribution that is obtained in various circuit designs.

X-filling methods are special optimization methods that put known binary values in don't-care bits of test patterns to reduce the number of signal transitions in scan operations. Large portions of a normal test pattern, known as don't-care bits, offer flexibility in assignment without affecting fault coverage [10]. With these bits strategically placed to align with values in neighboring scan cells, the number of transitions during a pattern shift is decreased directly, and dynamic power consumption is decreased. The optimization task aims to find assignments that reduce Hamming distances among sequential scan cell values, thereby generating less coarse data patterns that result in fewer switching events during the operation of the scan chain.

The use of don't-care bit assignment strategies balances the various targets, such as minimizing transitions, compression efficiency and preservation of fault coverage [8]. Greedy algorithms apply don't-care values to attempts to minimize transition counts in the current position, whereas global optimization methods apply implications globally on the choices of assignment patterns. Standard Frequency-Directed Run-Length compression is effective, achieving between 43.26% and 81.30% compression, while Golomb coding reaches 40.70 Compression and X-filling are sensitive to each other: aggressive compression can limit the flexibility of don't-care bits, preventing transition reduction. Successful implementations combine the techniques, using compression to decrease the total data volume while using the unused don't-care bits to optimize power.

Reduced switching activity in scan operations goes beyond optimizing individual patterns to include test sequence sorting and pattern generation algorithms. Rearranging pattern sequences minimizes power usage during transitions between test vectors [9]. The S13207 circuit always achieves the highest compression ratios with all encoding methods, showing that the features of the patterns greatly affect how well encoding works. The power awareness pattern generation algorithms generate test sets that meet coverage goals and naturally result in fewer transitions than non-power pattern generation methods. These algorithmic boosts are used to supplement architectural power reduction schemes, forming extensive structures that deal with power use in all aspects of test data handling.
CompressionWhen developing the test, it is crucial to thoroughly consider the trade-offs between compression and fault coverage [10]. Compression ratio, power reduction, and coverage assurance are the three factors that determine the practical compression strategies that can be adopted in production testing situations where quality standards are paramount regardless of power management goals.

ISCAS Circuit	Original Test Data (bits)	Extended-FDR Compression (%)	FDR-Compression (%)	Golomb-Code Compression (%)
S5378	23,754	56.38	48.02	40.70
S9234	39,273	53.37	43.59	43.34
S13207	165,200	85.55	81.30	74.78
S15850	76,986	71.90	66.22	47.11
S38417	164,736	65.84	43.26	44.12
S38584	199,104	66.67	60.91	47.71

Table 2: Test Data Compression Effectiveness [8]

ISCAS circuit measurements measure the performance of the compression methodology in various encoding schemes. Extended Frequency-Directed Run-Length coding achieved 53.37%-85.55% compression based on circuit design [8]. The compression of the Standard Frequency-Directed Run-Length was 43.26%-81.30%, and Golomb coding was 40.70%-74.78%. It was found that the S13207 circuit produced maximum compression in each of the

methods tried, implying pattern characteristics influence successful encoding. Findings affirm compression techniques in minimizing test data volume.

5. Voltage and Frequency Management in Test Environments

Low-voltage testing methodologies provide convenient methods for power reduction, where integrated circuits are tested with supply voltages lower than nominal in test conditions. The basic concept plays off the quadratic dependence between the supply voltage and dynamic power consumption, where small voltage decreases generate large power savings. Reduced voltage testing reduces switching currents and voltage swings across parasitic capacitances, which reduce scan operation energy dissipation and capture events. A detailed characterization is needed during implementation to define minimum voltage levels to ensure that the circuit functions and provides sufficient timing margins to ensure the reliable detection of faults in all test patterns.

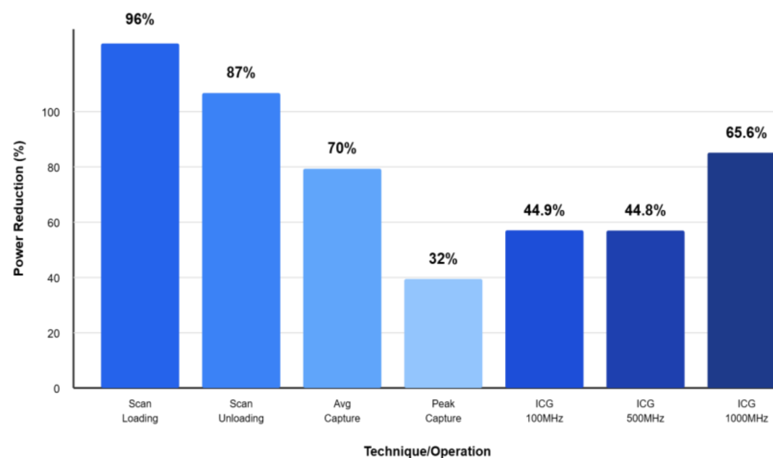
The benefits of supply voltage reduction go beyond the immediate savings of power to pressure on the thermal stress of the power-delivering networks. Reduced operating voltages produce lower levels of heat during active test phases, meaning that thermal constraints that would otherwise limit test parallelism or cause long cooling periods between test insertions are not a significant issue. The network of power supply networks will have less current demand at lower voltages, and this reduces the effects of voltage drops and bouncing of ground with respect to the networks, thus reducing test accuracy. These secondary benefits add to the effect of direct reduction of power, generating overall improvements in the management of the test environment.

Maintenance Fault coverage operation under lower voltages is a challenge that needs confirmation that the defect detection limits are not impaired by the changed conditions of operation. Some types of faults have the property of being voltage-dependent detections such that lower supply levels can obscure defects that would be detected at the nominal voltages, or higher voltages can detect marginal defects not detected at normal conditions. Complete test programs should confirm the adequacy of coverage at the desired voltages and may enhance low-voltage testing with nominal voltage testing of class-critical faults. The validation phase makes sure that power optimization does not accidentally reduce the quality levels or test escapes are created.

Dynamic voltage and frequency scaling Dynamic voltage and frequency scaling applications are uses of supply conditions that vary in real-time over the test run, optimizing the power consumption according to the current workload requirements. This adaptive strategy acknowledges that various test phases have different computational demands, and some operations can be run with reduced performance, whereas others need to be run in full-speed. Scaling algorithms check the test progress and change the voltage-frequency pairs to accommodate the current operational requirements, with sufficient performance margins at the lowest possible energy cost. This approach is a dynamic one, whereas low-voltage testing that is not dynamic is a static one, and the dynamic nature of this approach provides more opportunities of finer grained optimization.

Real time adjustment schemes in testing are based on hardware support of fast switching of voltages and software synchronization to compromise scaling decisions with the order of test sequences. The newer test equipment uses programmable power supplies that can change voltage in a microsecond or even in a single pattern, allowing scaling to be made with test pattern limits, or even inside a pattern. Control algorithms examine future test needs to pre-calibrate conditions to prevent performance bottlenecks and optimize power savings in periods with reduced load. This integration between intelligent control and hardware abilities produces reactive power management systems.

Workload optimization strategies segment the test operations on the basis of their power and performance requirements and use the correct voltage frequency combinations in each category. Scan shift operations, which are operations of simple propagation of data that do not involve elaborate logic evaluation, are aggressive-scale tolerant, unlike capture operations that would demand full-speed fault activation. Pattern-specific analysis provides the opportunities of customized voltage frequency assignments, to establish test schedules that trade off completeness and power limits. Circuit specific voltage and frequency tuning, design variations, corners of processes and temperature conditions are considered and hence all variations of manufacturing are guaranteed to work reliably across the manufacturing variations and maximum practical power reductions are achieved. It involves only minor hardware changes to integrate with preexisting test infrastructures and largely hardware changes are limited to software additions to test program generation and test execution control systems.



Graph 1: Clock Gating Power Reduction [2, 3]

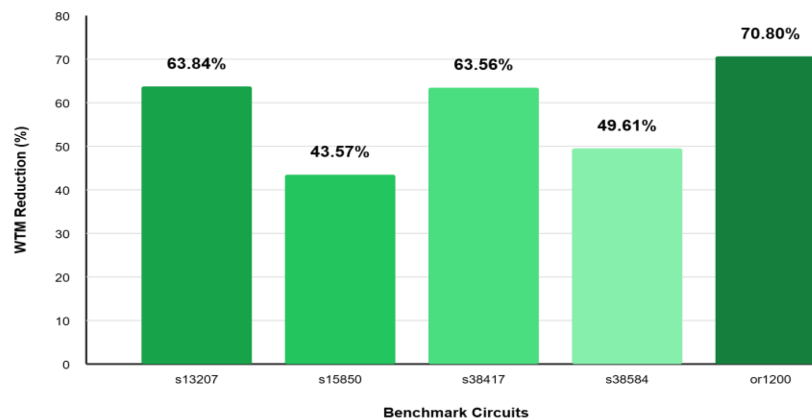
The graphical representation shows the power reduction magnitudes in different clock gating implementations at the test operations. When using clock gating cells, scan loading and scan unloading have the greatest reduction of 96 and 87% respectively [2]. Operation capture demonstrates 70% average reduction and 32% maximum reduction. Intelligent clock gating demonstrates only slight variation between 100 MHz and 500 MHz at 44.9% and 44.80 respectively, whereas the performance rises by far to 65.60 percent when it is operated at 1 GHz [3]. The data validates frequency-related power savings, where the greater the operation frequency, the greater the percentage of reduction.

6. Advanced Scan Chain Optimization Methods

Scan chain segmentation Architectures divide long scan chains into small independent segments that can be operated independently in a test run. This architectural change allows selective activation of chain segments and minimizes activated flip-flops at any given time during scan operations [4]. Segmentation boundaries are placed so as to match natural circuit boundaries in a strategic way to minimize the routing overhead and maximize power reduction opportunities. The independent control of segments enables segments of scan chains to be held inactive in test phases where they are not required in fault coverage goals.

Power reduction techniques based on selective capture aim at the capture stage of scan testing where circuit responses to test stimuli are loaded into scan cells. The classical models represent all the flip-flop states at once and generate power peaks which put strain on circuits and delivery networks [5]. Only those subsets of flip-flops needed to detect certain faults are activated by selective capture and the rest are kept inactive. Such selectivity minimizes instantaneous switching activity on capture events, decreasing peak power but maintaining full fault coverage via multi-capture cycles.

Scan cell reordering is used in transition minimization in shift operations where the highly correlated cells are placed next together in the scan chains. Correlation is a method used to examine the properties of a test pattern that determines patterns of cell pairs that have a similar value sequence across pattern sets [7]. Co-locating correlated cells in a scan chain ordering minimizes switching in pattern shifting, with benchmark circuits demonstrating Weighted Transition Metric reductions ranging from 43.57% to 70.80% depending on circuit characteristics [7]. The graph-based algorithms find the best possible cell ordering that will minimize the total number of transitions being made whilst still taking into account physical design constraints. The or1200 circuit achieves maximum optimization at 70.80%, while circuits s13207 and s38417 demonstrate similar performance at 63.84% and 63.56% respectively [7]. The high fault coverage preservation schemes maintain that power optimization schemes do not affect defect detection schemes which confirm that coverage measures do not fall short of industry tool standards of more than ninety-five percent of all fault models. Circuit s38584 exhibits moderate performance at 49.61%, whereas s15850 shows the lowest reduction at 43.57% among evaluated benchmarks, suggesting that larger designs benefit more substantially from scan chain reordering techniques [7].



Graph 2: Scan Chain Optimization Performance [7]

Evaluations of benchmark circuit mode measure the effectiveness of scan chain optimization by measuring the reduction of Weighted Transition Metric. The or1200 circuit is optimized to the maximum at 70.80, which is better in terms of optimization capacity [7]. Circuits s13207 and s38417 have similar performance with 63.84% and 63.56% respectively, whereas 38584 has a moderate performance with 49.61%. The lowest reduction of 43.57% among the benchmarks considered is captured in circuit s15850. This change amongst circuits suggests that the characteristics of the circuit and the ability to optimize the circuit are correlated with the size of the design, and the larger the design, the larger the advantage of scan chain reordering techniques should be.

Conclusion

Power-aware Design like methodologies are the fundamental structures of addressing the energy requirements in the current integrated circuit testing processes. Clock gating, partitioned testing, test data compression, voltage management, dynamic scaling, scan chain optimization and other key components can be used to ensure that semiconductor manufacturers can save significant costs and also increase the reliability of the devices during the production stages. These methods show that the decrease in power consumption at any point of testing is not accompanied by fault coverage or detection deficiencies, when properly applied. The article touches upon the key manufacturing issues such as thermal management issues, the device longevity issues, the optimization of the operational expenses, and the environmental sustainability goals in the form of reduced energy consumption. With the process technology on semiconductor technologies moving toward smaller process nodes and enhanced transistor densities, the importance of power-conscious testing strategy is becoming ever more important. Some of the future research directions include machine learning algorithms that assist in the intelligent generation of test patterns, investigation of adaptive power management schemes of heterogeneous chip design, development of cross-domain optimization strategies that are able to assist in achieving more than one power reduction objective, and development of industry-standardized frameworks that will enable the widespread adoption of power-aware Design for Test practices. Further development of these techniques will come in handy in ensuring the ability of producing semiconductors in a sustainable manner without compromising high quality standards necessary in the manufacture of electronic systems nowadays.

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